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ANALYSIS OF PD, POD, APOD, CO AND VF PWM TECHNIQUES FOR CASCADED INVERTER

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Abstract:

This paper presents multicarrier PWM strategies for three phase cascaded multilevel inverter. Multilevel inverters posses the advantage of reduced harmonics, high-power capability and high-voltage level. This paper focuses on multicarrier space vector pulse width modulation (MCSVPWM) strategy for the three phase multilevel cascaded inverter. A simulation model of three phase cascaded inverter developed using MATLAB/SIMULINK and its performance has been analyzed.
Keywords: SVPWM, PD, POD, APOD, CO, VF
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INTRODUCTION

Multilevel inverter has drawn tremendous interest in high power applications because it has many advantages: it can realize high voltage and high power output through the use of semiconductor switches without use of transformer and without dynamic voltage balance circuits. When the number of output levels increases, harmonics of the output voltage and current as well as Electro Magnetic Interference (EMI) decrease. The multilevel Inverter using cascaded-inverter with separate DC sources (SDCSs) synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. A three -phase 7- level configuration of such an inverter is shown in Fig. 1 Each SDCS is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S1-S4, each inverter level can generate three different voltage outputs, +Vdc, -Vdc, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. In this topology, the number of output phase voltage levels is defined by $m = 2s+1$, where s is the number of dc sources. A 7-level cascaded-inverters based inverter, for example, will have three SDCSs and three full-bridge cells. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter levels. For a three-phase system, the output voltage of the three cascaded inverters can be connected in either Wye or Delta configuration. Multilevel inverter can be defined as a device that is capable to produce a stepped waveform.

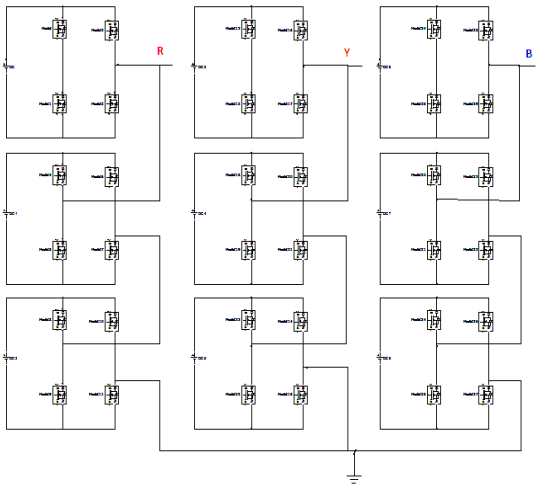

Fig: 1 Simulink Model of Cascaded Seven Level Inverter

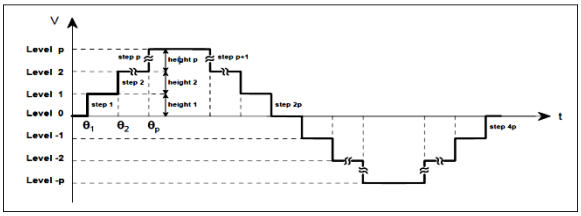

Fig : 2 Seven Level Output Waveform

P: number of steps in a quarter cycle;
2*p+1: number of levels of a converter;
4*p: **number** of steps of a converter.

In the generalized waveform, both width and heights of the steps can be adjusted. However, heights of steps are usually made equal and only widths are adjusted according to the desired waveform shape. It this case, a multilevel waveform is fully characterized by its 'p' stepping angles. ($\theta_{1,}\ \theta_{2,..}\ \theta_{p)}$

SPACE VECTOR PWM

The space vector PWM (SVPWM) is an alternative method used to control three-phase inverters, where the PWM duty cycles are computed rather than derived through hardware comparison like sine-triangle PWM. In SVPWM [3], [4], the three-phase stationary reference frame voltages for each inverter switching state are mapped to the complex two-phase orthogonal α-β plane. The reference voltage is represented as a vector in this plane and duty-cycles are computed for the selected switching state vectors n^{th} number of switching state vectors increases and this additional complexity has prompted many attempts at optimizing the performance of the SVPWM method for multilevel inverters.

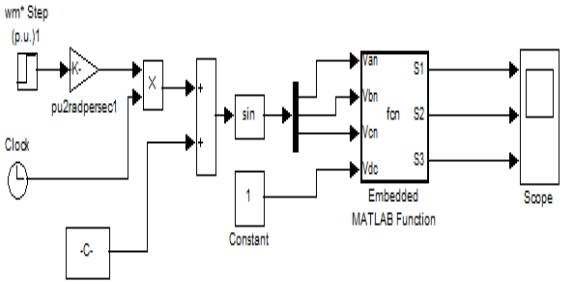

Fig: 3 Simulink Model of the SVPWM Generator

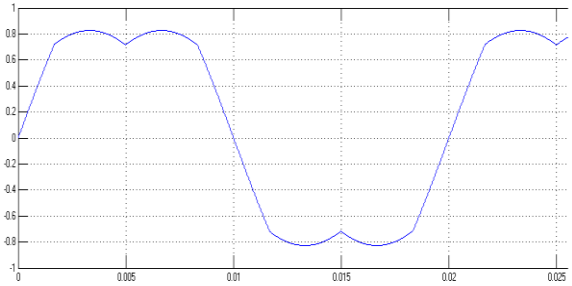

Fig: 4 Output Waveform of SVPWM

The principles of carrier-based PWM that are used for multilevel inverter. This paper focuses on carrier based PWM techniques which have been extended for use in multilevel inverter topologies by using multiple carriers. Multilevel carrier based PWM methods have more than one carrier that can be [4] triangular waves or saw tooth waves and so on. One of the most straightforward methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms.

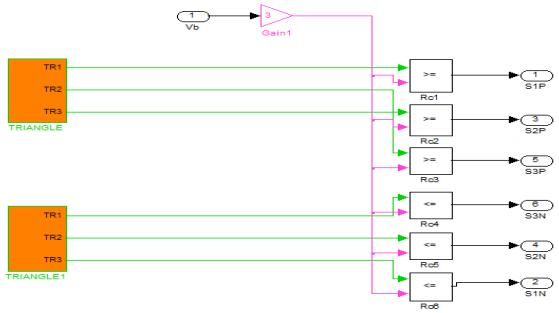

Fig: 5 Simulink Model Developed for Three Phase SVPWM Strategy by Triangle Waveform

MULTICARRIER PWM STRATEGEY

There are five alternative PWM strategies with differing phase relationships [4], [5]:

- Alternate phase disposition (APOD) – every carrier waveform is in out of phase with its neighbour carrier by 180 degree.
- Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are 180 degree out of phase with those below zero.
- Phase disposition (PD)-All carrier waveforms are in phase.
- Carrier over lapping (CO) – one or more carrier waveforms overlap with each other.
- Variable frequency (VF) – time duration of the one or more waveforms will vary.

3.1 Phase Disposition (PD)

The Carrier-based implementation the phase disposition PWM scheme is used. Fig.5 demonstrates the sine- triangle method for a seven-level inverter. Therein, the R-phase modulation signal is compared with six (m-1 in general) triangle waveforms.

The rules for the phase disposition method, when the number of level m = 7, are

- The m –1 = 6 carrier waveforms are arranged so that every carrier is in phase.
- The converter is switched to + Vdc / 2 when the reference is greater than both carrier waveforms.
- The converter is switched to 0 when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
- The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

In the carrier-based implementation at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the definition of the switching pulses is generated.

Amplitude of modulation index $m_a = 2 A_m / (m-1) A_c$

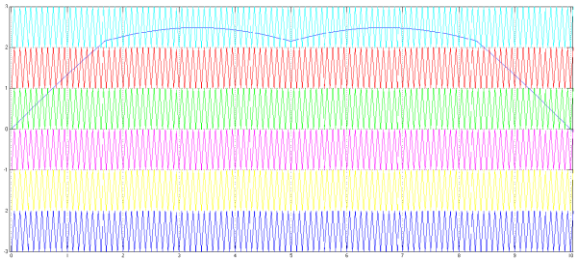

Fig: 6 Carrier arrangement for PDPWM (ma=0.8) with SVPWM reference

3.2 Alternate Phase Disposition (APOD)

In case of alternate phase disposition (APOD) modulation [4], [5], every carrier waveform is in out of phase with its neighbour carrier by 180 degree. Since APOD and POD schemes in case of seven-level inverter are the same, a seven level inverter is considered to discuss about the APOD scheme.

The rules for APOD method, when the number of level m = 7, are

- The m – 1 = 6 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbour carrier by 180degree.
- The converter switches to + V_{dc} / 2 when the reference is greater than all the carrier waveforms.
- The converter switches to +V_{dc} / 4 when the reference is less than the uppermost carrier waveform and greater than all other carriers.
- The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lowermost carriers.
- The converter switches to - V_{dc} / 4 when the reference is greater than the lowermost carrier waveform and lesser than all other carriers.
- The converter switches to -V_{dc} / 2 when the reference is lesser than all the carrier waveforms.

Amplitude of modulation index $m_a = 2 A_m / (m-1) A_c$

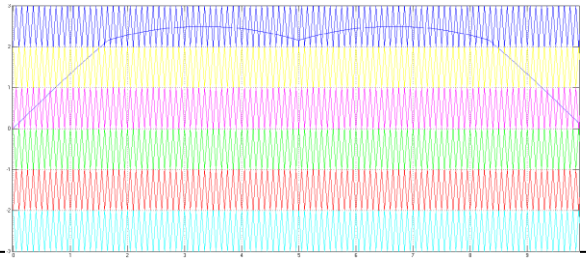

Fig: 7 Carrier arrangement for APODPWM (ma=0.8) with SVPWM reference

3.3 Phase Opposition Disposition (POD)

For phase opposition disposition (POD) modulation [4],[5] all carrier waveforms above zero reference are in phase and are 180 degree out of phase with those below zero.
The rules for the phase opposition disposition method, when the number of level m = 7 are

- The m –1 = 6 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180 degree out of phase with those below zero.
- The converter is switched to + V_{dc} / 2 when the reference is greater than both carrier waveforms.
- The converter is switched to 0 when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
- The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

Amplitude of modulation index $m_a = 2 A_m / (m-1) A_c$

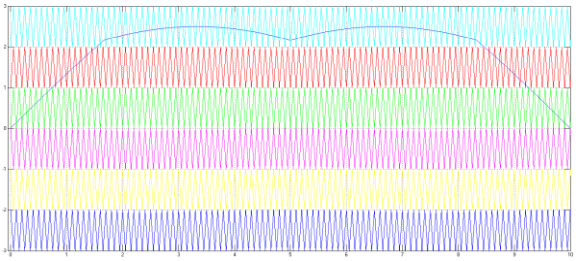

Fig: 8 Carrier arrangement for PODPWM (ma=0.8) with SVPWM reference

3.4 Carrier Overlapping PWM (COPWM)

For an m-level inverter[4], [6] using carrier overlapping technique, m-1 carriers with the same frequency fc and same peak-to-peak amplitude Ac are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is Ac/2. The reference waveform has amplitude of Am and frequency of fm and it is centered in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier Comparative Study on Carrier Overlapping PWM Strategies for Five signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off.

Amplitude of modulation index

$$m_a = A_m / 2A_c$$

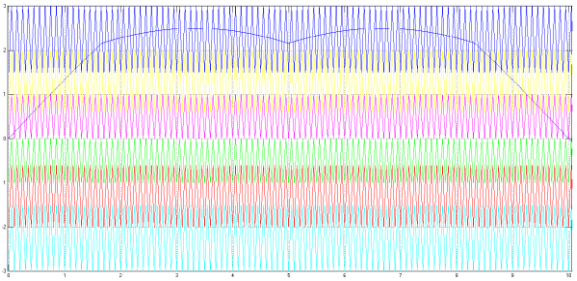

Fig: 9 Carrier Arrangement for COPWM (ma=0.8) with SVPWM Reference

3.5 Variable Frequency PWM Strategy (VFPWM)

The number of switching for upper and lower devices of chosen MLI is much more than that of intermediate switches in other PWM using constant frequency carriers. In order to equalize the umber switching for all the switches, variable frequency

PWM strategy is used [4].

Amplitude of modulation index $m_a = 2 A_m / (m-1) A_c$

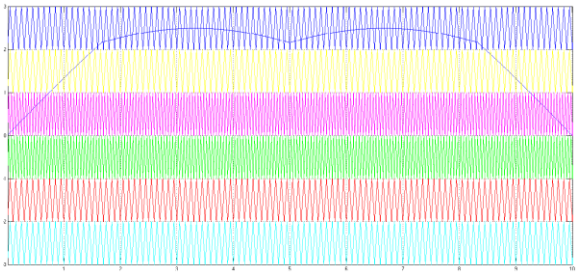

Fig: 10 Carrier arrangement for VFPWM (ma=0.8) with SVPWM reference

I. SIMULATION RESULTS

The cascaded seven level inverter is modelled in simulink using power system block set. Switching signals for cascaded multilevel inverter using MCSVPWM strategies are simulated. Simulations are performed for different values of m_a ranging from 0.8 to 1 and the corresponding %HTD are measured using the FFT block and their values are listed in table I. Figure 11-20 shows the simulated output voltage of cascaded multilevel inverter and their harmonic spectra. The following parameter values are used for simulation: V1= 50V, V2=50V, V3=50V, R (load) = 100 Ohm, Fc=10000Hz and Fm=50Hz.

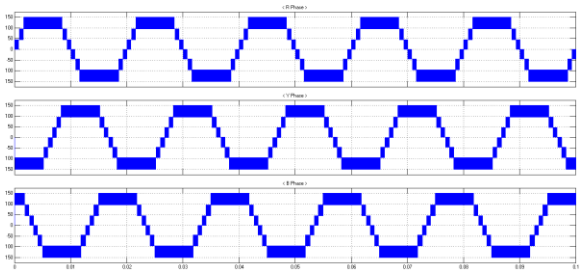

Fig: 11 Output Voltage Generated by PDPWM

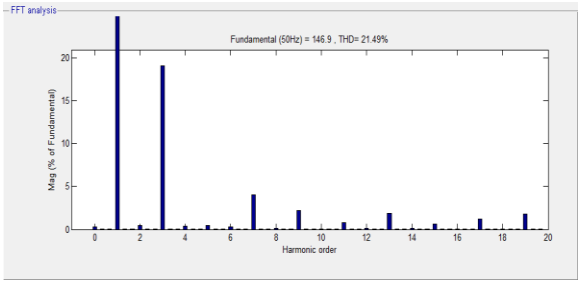

Fig: 12 FFT Plot for Output Voltage of PDPWM

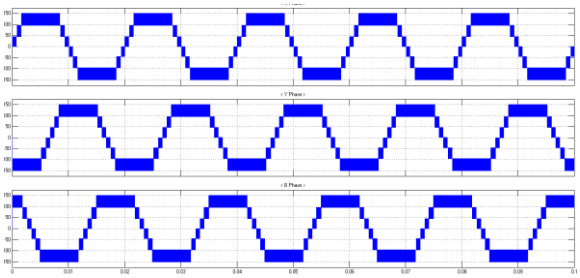

Fig: 13 Output Voltage Generated by PODPWM

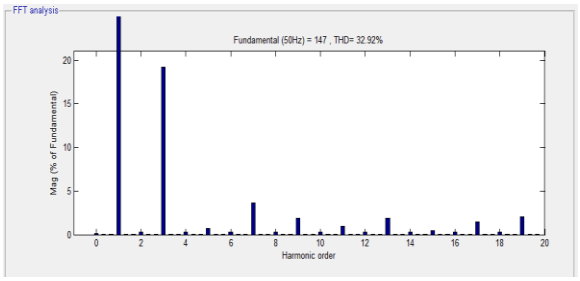

Fig: 14 FFT Plot for Output Voltage of PODPWM

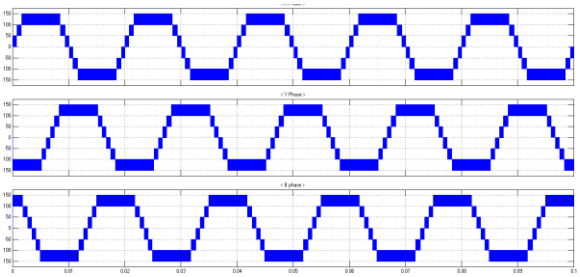

Fig: 15 Output Voltage Generated by APODPWM

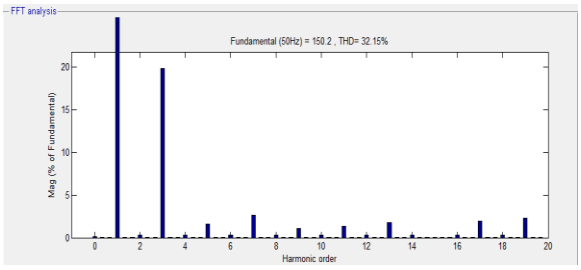

Fig: 16 FFT Plot for Output Voltage of APODPWM

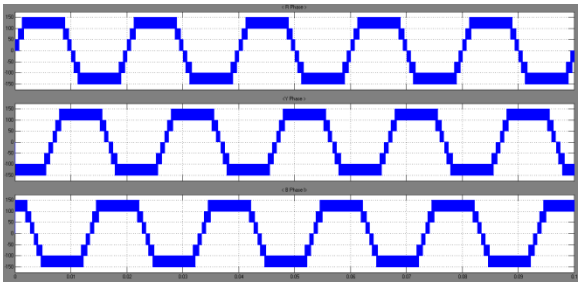

Fig: 17 Output Voltage Generated by CODPWM

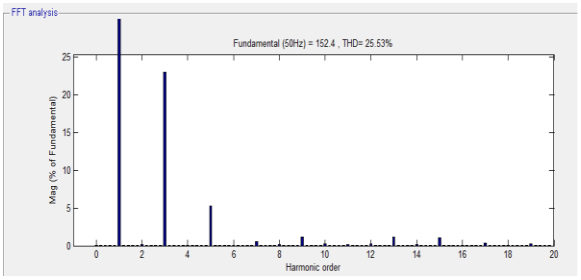

Fig: 18 FFT Plot for Output Voltage of COPWM

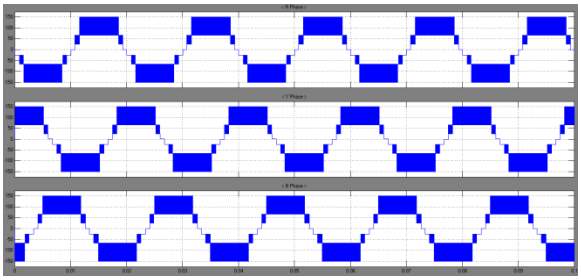

Fig: 19 Output Voltage Generated by VFPWM

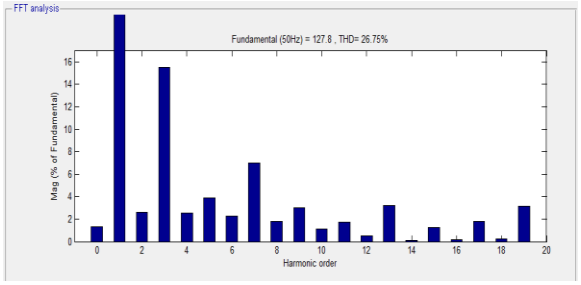

Fig: 20 FFT Plot for Output Voltage of VFPWM

Table-I % THD for Different Modulation Indices

ma	PD	POD	APOD	CO	VF

1	21.39	33.36	32.23	25.18	26.83
0.8	23.44	34.28	33.49	27.20	27.62
0.9	25.69	35.93	34.79	28.78	28.91

Table- II VRMS (Fundamental) for Different Modulation Indices

ma	PD	POD	APOD	CO	VF
1	146.3	147	150.2	152.4	127.8
0.8	142.1	133.4	139.8	141.3	140.6
0.9	137.5	130.1	132.3	136.5	135.1

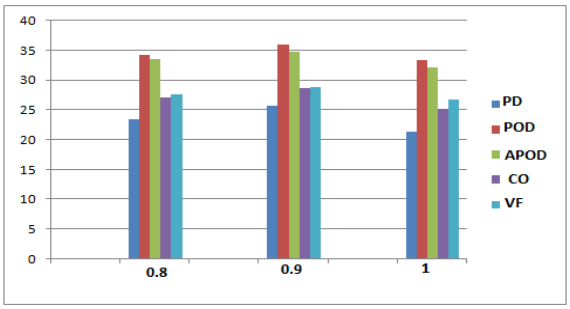

Fig 21: % THD vs Modulation index (ma)

II. CONCLUSION

In this paper, MCSVPWM strategy for three phase seven level cascaded inverter has been presented. Performance factors like % THD and VRMS have been measured, presented and analyzed. It is found that the PDPWM strategy provides lower %THD and higher VRMS and less number of dominant harmonics than the other strategies. In the future scope DC source can be replaced by renewable energy sources and the seven level cascaded inverter can be used for distributed generation systems.

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