SAJET

South Asian Journal of Engineering and Technology Vol.2, No.18 (2016) 71–77

**ISSN No: 2454-9614**

# A Survey on the Performance Analysis of 6t Sram Cell Using Novel Devices

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**Received: 10/11/2015, Revised: 13/12/2015 and Accepted: 07/03/2016**

**Abstract**

Static Random Access Memory (SRAM) continues to be a critical component across a wide range of microelectronics applications from consumer wireless to high performance processors, multimedia and System on Chip (SoC) applications. As the technology scales down to 32nm and below, the leakage power of Static Random Access Memory (SRAM) are becoming one of the most critical concerns for low power applications. Scaling causes severe Short Channel Effects (SCE) which are difficult to suppress them. To overcome the challenges in nanometer region, many alternate devices like Multi, Gate Field Effect Transistor (MuGFET), Fin-shaped Field Effect Transistor (FinFET), Carbon Nano Tube Field Effect Transistor (CNTFET) and Tunnel Field Effect Transistor (TFET) are used in conventional 6T SRAM cell design. The performance parameters like standby power, dynamic power, write delay, read delay and static noise margin are compared using 32nm technology for the various devices.

*Keywords - CMOS, FinFET, CNTFET, TFET, Standby Power Consumption, Static Noise Margin*

**Reviewed by* **ICETSET'16** *organizing committee*

## 1. Introduction

The demand for low-power design and design trend is to increase the speed and working frequency of digital systems. Recently, some applications such as wireless sensor network, portable and battery-operated applications which involve SRAM as its major portion of its chip demand low power operation. As the MOSFETs are scaled down to nano-scale regime, statistical dopant fluctuations, oxide thickness variations and line edge roughness to increase the spread in transistor threshold voltage ($V_{th}$) and correspondingly affect the "on" and "off" currents **[1]**. At sub-32nm channel lengths, achieving a large current drive while maintaining a low off-state leakage becomes difficult. To solve this problem new technology MOSFET architectures involving the use of multiple gates controlling the transistor have been proposed. The FinFET device (is a self-aligned double-gate MOSFET), CNTFET devices contain a straightforward process flow when starting from a conventional CMOS bulk transistor.

Steep sub threshold slope TFET, which utilizes the conduction mechanism in band-to-band tunneling, is one of the most promising candidates for ultra-low voltage/power applications.All these devices are used for the construction of the conventional 6T SRAM cell and its effect on various parameters are being studied in this paper.

## 2. SRAM CMOS cell design problems

The classical bulk-Si MOSFET structure down into the sub-20nm regime, SCE control requires heavy channel doping (>$10^{18}$ $cm^{-3}$) and heavy super-halo implants to control sub-surface leakage currents. As a result, carrier mobility's are severely degraded due to impurity scattering and a high transverse electric field in the on-state. The off-state leakage current specification and on-state drive current is degraded. Off-state leakage current is enhanced in the band-to band tunneling between the body and drain. Vth variability caused by random dopant fluctuations is another concern for nano-scale bulk-Si MOSFETs **[2].**

In a bulk MOSFET based SRAM array is exponential increase the leakage current, the standby power becomes larger.Increasedtransistor leakage and parameter variation present challenges for scaling of CMOS conventional six-transistor (6-T) SRAM cell as shown in figure 1. Reduction in power dissipation can be achieved by reducing the power supply voltage, but this has a disadvantage of increasing the delay. The CMOS cell fails to assemble the operational requirements due to the low read Static Noise Margin (SNM).To overcome these difficulties, optimization of the device structure is very important for low-power and robust SRAM cell design in sub- 32 nm using CMOS, FinFET, CNTFET, TFET technologies.

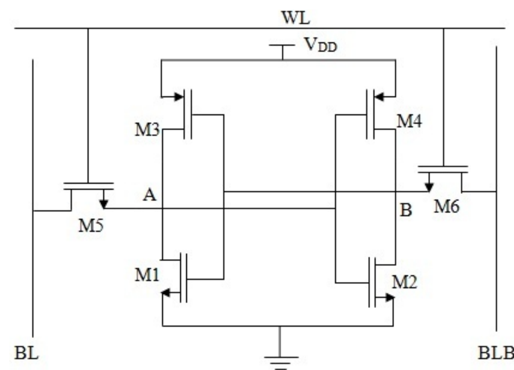


Fig .1The conventional 6T SRAM cell.

## 3. Novel devices based SRAM design

### *3.1 FinFET Technology*

FinFETs are double-gate field-effect transistors that are able to overcome these scaling obstacles **[3].** The electrical coupling between the front and back gates is a unique property of the FinFET technology. The inference of this coupling is that the threshold voltage of the front gate ($V_{thf}$) is not only established by the process, but it can be

controlled by the Back Gate Voltage ($V_{Gb}$). This is similar to the body effect in a bulk transistor.The characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon “fin”, the body of the device is formed. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. Figure 2, Shows the structure of a multi-fin double gate FinFET device. Current flow is parallel to the wafer plane.

Proper optimization of the FinFET devices is necessary for reducing leakage power and improving stability in 6T SRAM **[7].** The supply voltage (VDD), Fin height (H fin) and threshold voltage ($V_{th}$) can be used to reduce the leakage power in FinFET SRAMs **[4].**

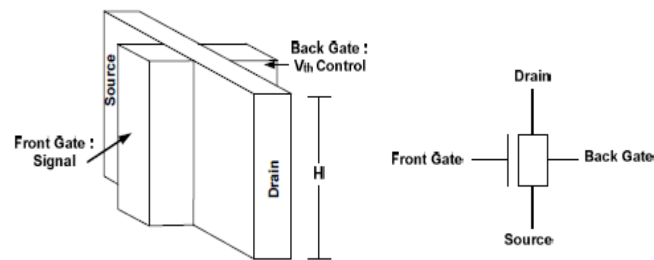


Fig. 2 FinFET Structure and Symbol.

However the leakage reduction in supply voltage has a physically powerful negative impact on the circuit cell stability under parametric variations [**5].** There is a requirement, a device optimization technique for FinFET to reduce leakage power and improve stability in an SRAM cell. Designing the SRAM cell with FinFET technology is adequate to read, write and static noise margins and lower power consumption. Decrease the delay at the cost of slightly increases the power dissipation in the SRAM cell. However to reduce power dissipation and leakage currents should be minimized **[6].**

FinFETs provide high drive current even with larger threshold voltage there by achieving high static noise margin (SNM) along with good write stability **[7].** RNM is often used as the measure of the robustness of an SRAM cell against flip during read operation. In read stability (High RNM) SRAM cell, pull down transistor is typically stronger than the access transistor. The read margin can be increased by the pull-down transistor in FinFET, which results in an area penalty and increasing the gate length of the access transistor, which increases the delay and hurts the write margin.

### *3.2 CNTFET Technology*

CNTFET is a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material as an alternative of bulk silicon in the traditional MOSFET structure. A single-wall carbon

nanotube (SWCNT) is a tube formed by the rolling of a single sheet of the grapheme. It can either be metallic or semiconducting depends on the chirality vector (m, n) therefore the direction in that the grapheme sheet is rolled. Semiconducting nanotubes contain attracted widespread attention of the electronic device and circuit designers as a promising channel material for high-performance transistors **[8].** The CNT channel region is undoped, and the other regions are heavily doped, acting as both the source and drain extension region and interconnects between two adjacent devices.

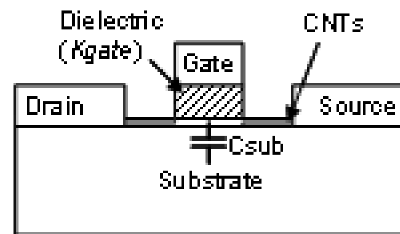


Fig. 3 CNTFET Structure.

Carbon nanotubes are high-aspect-ratio cylinders of carbon atoms. The electrical property of the single wall carbon nanotube (SWCNT) offers the potential for molecular-scale electronics. A feature semiconducting single-wall carbon nanotube is 1.4nm in diameter with 0.6 eV band gap energy (is inversely proportional to the diameter).The Recent carbon nanotube field effect transistors (CNTFETs) have a metal carbide source and drain contact **[9]** and a top gated structure (Figure 3) with thin gate dielectrics **[10].** The sub threshold slope and contact resistance are equal to the silicon FET. Since the nanotube diameters are fixed, the CNTFET is constructed as an array of carbon nanotubes which occupy equal lines and spaces.

The CNTFET has a considerably higher on-off current ratio compared to the MOSFET in the deep sub-micron range. In CNTFET standby power of the SRAM cell is very low compared to its CMOS technology at a power supply of 0.9V. The leakage power CMOS is 46 times larger than the value for the CNTFET SRAM cell. Dynamic power dissipation of CNFET becomes greater as VDD increases as the dynamic power difference between the 6T SRAM cells. CNTFET have the highest SNM because of the relatively higher threshold voltage and lower leakage current than CMOS cells. The write margin of CNFET cell is lower than the CMOS cell **[11].**The CNTFET to reduce the write-power dissipation and to reduce the read delay.

### *3.3 TFETechnology*

The TFET (Tunneling Field Effect Transistor) acts as field-effect transistor, whereas changing the gate voltage turns the current ON and OFF, but which uses band-to-band tunnelling (BTBT) in the transition between the channel and source region. The simplest version of a TFET is produced by inverting the n-type source region into the p-type as shown in Figure 4. TFET is a bipolar device, it will show P-type behavior with dominant hole conduction.

Besides that also vertical TFETs have been presented [12]. These devices have the potential for very low OFF-current and offer the possibility to lower the sub threshold swing below the 60 mV/decade limit of conventional MOSFETs. They offer the opportunity for an extreme reduction of sub threshold leakage compared to conventional CMOS technology. However, the experimentally shown ON-currents are significantly below the values achieved with the MOSFETs.

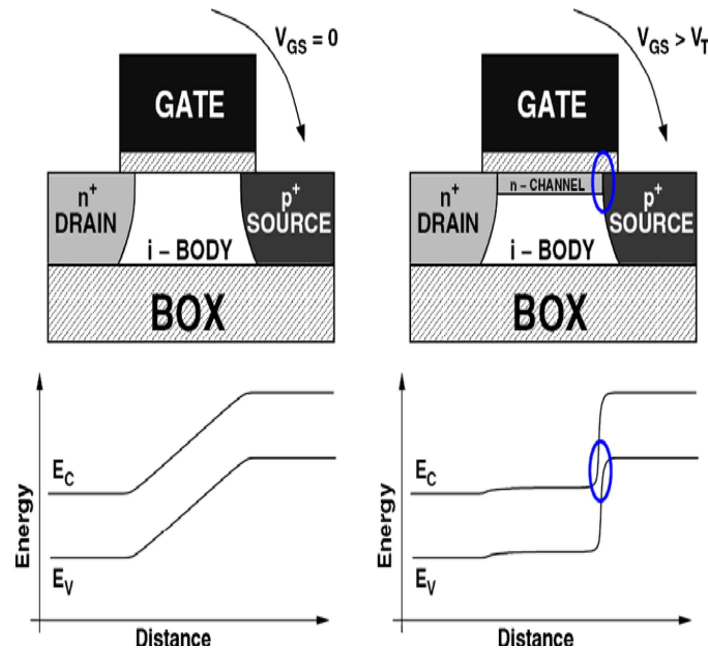


Fig 4: The Cross-section of an SOI Tunneling Field Effect Transistor and band diagrams for OFF and ON states.

TFET SRAM has better performance and reliability than CMOS SRAM cell **[13, 14]** and it occupies less area and consuming at smaller amount 4 orders of magnitude lower static power than the TFET SRAMs in **[13]** and **[14]** respectively. Further, it not only like a comparable performance and reliability to the 32nm 6T CMOS SRAM, but also consumes 6–7 orders of magnitude of static power are lower, making it attractive for low-power, high density SRAM applications.For the write delay, the 6T CMOS SRAM has a smaller delay than all the TFET SRAMs over most supply voltage. The 6T CMOS SRAM has the smallest read delay, yet the proposed 6T TFET SRAM still out performs other TFET SRAM. Using this design strategy, the proposed 6T TFET SRAM achieves reliability and best performance as well as the minimum dynamic power and leakage power in comparison to existing TFET SRAM.

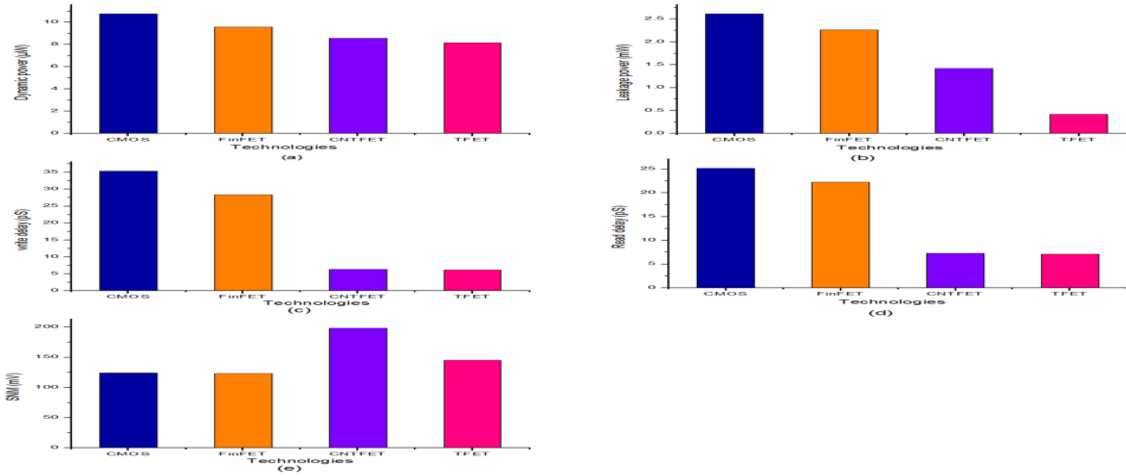


Fig. 5(a) Dynamic power (b) Leakage power (c) Write delay (d) Read delay (e) SNM

The simulation result for various parameters of 6T SRAM Cell using CMOS, FinFET, CNTFET and TFET is shown in table1.

Table 1
Summarized simulation results

| Parameters | CMOS | FinFET | CNTFET | TFET |
|---|---|---|---|---|
| Dynamic power(μw) | 10.75 | 9.57 | 8.56 | 8.16 |
| Leakage power (nw) | 2.61 | 2.26 | 1.42 | 0.42 |
| Write delay (ps) | 35.34 | 28.32 | 6.31 | 6.12 |
| Read delay (ps) | 25.14 | 22.25 | 7.25 | 7.12 |
| 1.1. SNM (mv) | 1.2. 124 | 1.3. 123 | 1.4. 198 | 1.5. 145 |

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***4.* Conclusion**

In SRAM, the leakage power has become a major issue in modern low power system on chip devices with technology scaling. This paper summarizes the performance of the 6TSRAMcellusing devices like CMOS, FinFET, CNTFET and TFET technology. From the comparison, it is clear that Tunnel FET exhibits less leakage power, dynamic power, wider SNM, read and write delay when compared with other devices in 32nm. In addition to memory design, all complex designs for other applications based on CMOS will be replaced CNTFET or FinFET or TFET in near future.

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